WHAT IS CLAIMED IS:

1. A fabricating method of a low temperature poly-silicon film, comprising:

forming an amorphous silicon layer on a substrate;

performing a first anneal treatment on the amorphous silicon layer, so as to covert the amorphous silicon layer into a poly-silicon layer wherein a plurality of mounds are formed on a surface of the poly-silicon layer, and an oxide layer is formed on the surface of the poly-silicon layer;

performing a surface treatment step on the poly-silicon layer, so as to remove the oxide layer; and

performing a second anneal treatment on the poly-silicon layer.

2. The fabricating method of the low temperature poly-silicon film of claim 1 wherein the surface treatment step is an etching treatment step.

3. The fabricating method of the low temperature poly-silicon film of claim 2 wherein the etching treatment step is performed by using a hydrofluoric acid solution.

4. The fabricating method of the low temperature poly-silicon film of claim 3 wherein the concentration of the hydrofluoric acid solution is from 1% to 15%, and the duration for performing the etching treatment step is from 1 minute to 15 minutes.

5. The fabricating method of the low temperature poly-silicon film of claim 1 wherein after the second anneal treatment is completed, the height/width ratio of the mounds on the surface of the poly-silicon layer is less than 0.2.

6. The fabricating method of the low temperature poly-silicon film of claim 1 wherein the first anneal treatment is a laser anneal treatment.

7. The fabricating method of the low temperature poly-silicon film of claim 1 wherein the second anneal treatment is a laser anneal treatment.

8. The fabricating method of the low temperature poly-silicon film of claim 1 further comprising a step of forming a buffer layer on the substrate before the amorphous silicon layer is formed on the substrate.

9. A low temperature poly-silicon thin film transistor (LTPS TFT), comprising:

a poly-silicon layer, deposited on a substrate, wherein the height/width ratio of a plurality of mounds on a surface of the poly-silicon layer is less than 0.2, and the poly-silicon layer comprises a source, a drain, and a channel that is deposited in between the source and the drain;

a gate isolation layer, deposited on the substrate, and covering the poly-silicon layer;

a gate, correspondingly deposited on the gate isolation layer that is deposited above the channel;

a dielectric layer, deposited on the gate isolation layer, and covering the gate;

a source metal layer, deposited on a surface of the dielectric layer and in the dielectric layer and the gate isolation layer wherein the source metal layer is electrically connected to the source; and

a drain metal layer, deposited on the surface of the dielectric layer and in the dielectric layer and the gate isolation layer wherein the drain metal layer is electrically connected to the drain.

10. The low temperature poly-silicon thin film transistor of claim 9, further comprising a step of depositing a buffer layer in between the substrate and the amorphous silicon layer.